Test Review

Test from last Thursday.

Biggest sellers of converters are HD to composite. All of these monitors in the studio are composite..

Identify the only portion of the vertical blanking interval waveform that is responsible for interlace.

Reference http://www.ntsc-tv.com/images/tv/RS-170A.gif

On odd line, the beginning of broad pulses starts at beginning of line 4. On even line, the beginning of broad pulses starts at middle of line 3. That is the beginning of interlace, the broad pulse of line 4 on the odd line.

The vertical sync pulses is made up of broad pulses. Why are there serrations? To maintain horizontal sync during the vertical interval. In some old TVs there are just broad pulses and no serrations, but there is the problem of **hooking** at the top of the picture due to horizontal oscillator getting out of sync due to no locking during the vertical interval.

The first pre-equalizing pulse within the half-line (last line of video).

The answer would need to include circling both the first broad pulse in the even line (the pulse that is at the middle of line 3) as well as the first broad pulse in the odd line (the pulse that is at the beginning of line 4).

Mark only the points of the supplied waveform that make up the hammerhead displayed above the waveform.

The answer to this will be contained within the lecture. The lecture and the answers to the quiz will be interspersed.

Lecture

First slide is where he got the picture for question 2. On the web at http://www.ntsc-tv.com/images/tv/hammer.gif

Top picture shows one line of video. Diagram 1 (just refer to the web GIF linked above – I can't show it in this document due to copyright restrictions since this document is on my web site). Equalizing pulses: the first one leading edge is at the same point as the leading edge of horizontal sync pulse. The 50% point of the falling edge is considered where sync starts. The equalizing pulse is ½ the width of normal sync pulse: 0.04 H – 2.542 microsecond. Vertical sync pulses still start at same point (the falling/negative-going edge).

The horizontal sections of this picture are aligned vertically with each other. This shows you correctly when the leading and trailing edges of the pulses occur within the lines, and it also is vertically aligned with the hammerhead display.

The equalizing pulses and serrations in the middle are completely ignored by the horizontal oscillator.

The pulses that make up the hammerhead are the bottoms of the pulses that fall within the middle of the lines shown.

The top of the hammerhead are the equalizing pulses that occur in the middle of lines 1, 2, and 3 on odd lines and (the last line of the previous even line) and lines1 and 2 on even lines.

Equalizing pulses are the pulses that make up the hammerhead; the other pulses are called **sync pulses**.

The portion of the head made up by the handle are the broad pulses that occur in the middle of lines 4, 5, and 6 on odd lines and 3, 4, and 5 on even lines.

The broad pulses are the two long horizontal black lines. They go into black for a long time.

Part of the linked diagram is wrong. The portion of the leftmost horizontal black line for the first broad pulses that lies just to the left of the front porch and start of the line should be white. It should be just like the end of the line shown, since that is where the serration is.

What is the purpose of the hammerhead itself?

Has no circuitry purpose. It's just for engineers to have a visual cue/symbol/placeholder when this is displayed on monitors.

What is the purpose of the black line before and after the hammerhead?

I'd word this "to the left and right" instead of "before and after". But, true, they are before and after *in time*, and to the left and right *within the diagram*.

It is the broad pulses, the vertical synchronizing signal.

On which line does burst start after vertical sync?

10.

What is the purpose of the circled equalization pulse in the above waveform?

It's the start of vertical blanking in that field. The monitor isn't looking for it. It's a visual indicator for engineers of the half-line shift. From the monitor's perspective, the field doesn't start until retrace completes. From the signal's perspective, the field starts there.

In the waveform at question 6, what effect on circuitry do every other equalization pulse have starting at the circled pulse?

Nothing (not to circuitry).

Why is there a need for vertical sync when we have so many horizontal syncs available?

Vertical retrace. To know where to start at the top in the monitor. Must be long enough to provide time for the vertical retrace to complete.

How many lines in the vertical interval?

20. Could be 21 or 22. Depends on what are counting.

Where on horizontal sync does retrace occur?

At the 50% point of the falling edge.

If just say retrace, implies horizontal retrace.

How does the hammerhead and all the other stuff in the vertical interval get displayed?

Steve thinks that the voltage/IRE of the signal gets raised so that it falls within the visible IRE range. It also theoretically could be that the monitor is modified to read lower IRE values as visible.

Interval Timings

Symbol	***Characteristics***	***Value***
v	Field period (ms)	16.6833
j	Field-blanking interval	(19 to 21) H + a
j'	Build-up time of the edges of field-blanking pulse (microseconds)	<= 6.35
K	Interval between front edge of field-blanking interval and front edge of first equalizing pulse (microseconds)	1.5 +/- 0.1
L	Duration of first sequence of equalizing pulses	3H
M	Duration of sequence of synchronizing pulses	3H
N	Duration of second sequence of equalizing pulses	3H
P	Duration of equalizing pulses (microseconds)	2.3 +/- 0.1
Q	Duration of field-synchronizing pulses (microseconds)	27.1
R	Interval between field-synchronizing pulses (microseconds)	4.7 +/- 0.1
S	Build-up time of synchronizing and equalizing	<= 0.25

The composite video signal is bipolar (has both positive and negative voltage parts) with a normalized signal amplitude of 1 V p-p. The 700 mV (714.3 mV) positive part of the signal conveys picture information. The negative part of the signal (285.7 mV) conveys synchronizing information. **Put this in black book**.

Vertical Blanking Interval

Occupies space equivalent to 9 lines in the vertical blanking interval (7.5 lines in the 625/50 format).

The vertical sync signal is composed of 6 (5 in PAL) short, 2.35 microsecond duration pre-equalizing pulses, followed by 6 (or 5) serrated vertical sync pulses (approximately 27 microseconds duration), followed by 6 (or 5) short, 2.35 microsecond duration post-equalizing pulses.

The serrations are needed to ensure continuing horizontal synchronizing during the vertical blanking period.

The relative complexity of the vertical synchronization is the price to pay for the reduced bandpass afforded by interlace.

Get better picture through interlace with lower bandwidth (which was the primary reason for interlacing, not due to the phosphor persistence), but got interframe jitter as a consequence (also flicker).

Burst

In addition to scanning synchronization information, chrominance subcarrier frequency and phase information is also transmitted as a burst of 9 +/-1 cycles (at 3.58 MHz in NTSC) or 10+/- 1 cycles (at 4.43 MHz in PAL). This information is required as a reference for the regeneration of the suppressed chrominance subcarrier used by the synchronous detector of the chrominance decoder.

This means that PAL has a bigger bandwidth than NTSC, since the subcarrier frequency is above our limited range of 4.25 MHz.

What happens to sync?

Receiver extracts the horizontal and vertical scanning information with a clipper with a threshold of 0V. Picture information is removed and sync is passed. We talked about transistors running at cutoff; this is how we separate sync out. The only time the transistor conducts is during sync.

The horizontal sync pulses pass through a differentiating circuit that generates short pulses coincident with the horizontal sync leading edge. These pulses feed to a PLL VCO to generate the horizontal scanning waveform.

The vertical sync pulses pass through an integrating circuit that removes the short duration horizontal sync and pre-equalizing pulses. The serrated pulses charge a capacitor to the value required to synchronize the vertical scanning generator.

The burst chrominance sync information is keyed out of the horizontal blanking interval and through a bandpass filter. The filtered bursts feed the PLL, crystal-controlled oscillator part of the chrominance decoder.

Diagram of camera outputting composite sync and active video, the sync separator in the monitor splits into horizontal and vertical sync.

Simple differentiating circuit to extract line sync pulses

See *diagram* 2.

Take a diode and cut off the positive-voltage spike generated from the rising edge. Left with the single spike generated by the falling edge, which goes into negative voltage.

Would have to amplify the signal in order for the diode to work, due to the 0.7V drop, so the signal must be at least 0.7V.

Generate a ramp for the deflection coil. See *diagram* 3. Use a linear portion of the RC curve. Every time we get to the top of that portion, we close a switch which shorts out the capacitor. This is how we get a ramp. Use transistors to short out the capacitor. Use biasing to set up into the linear portion of the RC curve.

Simple integrating circuit to extract vertical sync pulses

See *diagram* 4. The differentiator and integrator diagrams are near the beginning within http://www.tek.com/Measurement/App_Notes/20_14229/eng/20W_14229_0.pdf

Once broad pulses come around, the integrator separates vertical sync from horizontal sync because the broad pulses result in enough of a voltage change to break through a clipping level.

Why equalization pulses were put in originally

Originally sync and equalization pulses same width. Pre-equalizing pulses prepared the monitor to see the broad pulses because it prepared the signal output from the integrator. Steve believes that is why they did this. Used to not have very well made capacitors; now they are made well. Old capacitors would age fast, and would not be precisely measured.

Discharge of the integrator happens continuously. It takes a lot of long pulses to get the integrator to keep enough charge.

Equalizing pulses are 2.3 microseconds –half of the width of horizontal sync pulses (4.7 microseconds).

NTSC Horizontal Blanking Interval (from SMPTE 170M)

This diagram is also in the above-mentioned PDF file on the web.

Genlock reference for analog video

The **black burst** signal is often used to genlock equipment. It is a composite signal that contains horizontal and vertical syncs and a small packet of NTSC or PAL color subcarrier (color burst). The term black burst arises from the fact that the active picture portion of the signal is at black level (0 mV for PAL, 7.5 IRE (black) for NTSC (America) and 0 IRE for NTSC no-setup (Japan)). The black burst is used for system timing, the sync is used for genlock and drive signals and the color burst is used for color framing reference.

Two types of sync. Comp sync runs about 4 volts, black burst is about 300 mV and it has sync on it. Why is comp sync so hot (at such a high voltage)? That's just the standard they started with, maybe to ensure it gets to the other end of the line.

Continuous Wave Sync Pulse Generator

A Continuous Wave (CW) signal may be used to genlock a **sync pulse generator** (SPG).

The CW signal is a sine wave clock signal, usually selectable between 1, 5, and 10 MHz. Start at high frequency, then divide it down to the frequency we need.

There is no positional information of H and V because it is only a clock.

The timing output of the SPG cannot be guaranteed if the CW signal is removed from the SPG and then re-applied.

High-definition (HDTV) analog horizontal timing

For high-definition *analog* horizontal timing, the HD tri-level sync is used instead of the bi-level sync pulse.

The reference point is at the blanking level on the rising edge, at the half height of the tri-level sync.

Diagram 5.

Why use tri-level sync instead of bi-level sync? The bi-level pulse really does offset our video, it forces us down to -40 IRE with nothing to balance us out.

No burst, no setup. There is a front porch and a back porch at 0 volts; these are short. The tips are at 300 mV and –300 mV.

This type of sync makes it very much easier to calculate an APL (average picture level) since the tri-level sync signal cancels with itself by adding up to zero.

Only Y has sync on it. R-Y and B-Y should not have any sync on them.

The tri-level sync signal has faster rise times because of the increased bandwidth of HD (by a factor of 3), which results in more accurate timing edges. Will have better square wave edges since don't have to cut off harmonics at as low a multiple of the fundamental frequency.

These factors also improve jitter performance and sync separation.

The Tri-level Sync Signal

Diagram 6.

HD sync

SMPTE 240.

Start at zero volts, first transition to -300 mV (+/- 6 mV) then transitions to +300 mV (+/- 6 mV), holds, then returns to zero or black level.

Display system looks for zero crossing of sync pulse. Each half of tri-level sync pulse defined to be 44 samples. Rise time defined as 4 samples wide +/- 1.5 samples.

One major advantage is symmetry of design resulting in net DC value of zero volts. That was the idea.

Bi-level signal introduces DC component into video signal.

Unique excursions of sync used in digital television derive numerical values that are easily coded and easily recognized within the digital transmission channel.

Diagram 7.

Why have no 7.5 setup and 0 blanking? No color subcarrier on high definition; put color in R-Y and B-Y. All video will be above blanking. No setup and no subcarrier on HD video.

High Definition Analog Vertical Timing

See that PDF doc.

Top one is progressive, middle one is interlaced first field, bottom one is interlaced second field.

Why still have interlaced? Get higher resolution within the limited bandwidth, as long as the subject isn't changing that much.

Digital Video Sync

There are no analog sync signals in digital video. Just use unique combinations of bit values to indicate stuff.

Exam

Be prepared for an exam on this stuff about vertical sync.