Phase Locked Loop

VCO = Voltage Controlled Oscillator – an oscillator controlled by a DC voltage.

Diagram 1.

Oscillation created by the LC tank circuit, being *tickled* by a little bit of positive feedback from the emitter to keep the oscillation going. Take the output from the collector.

To make a VCO, put a **varactor diode** in place of the capacitor. Changing capacitance (by changing the DC voltage on the varactor) changes the resonant frequency of the tank circuit.

Why would someone want to change the resonant frequency? For example, tuning a radio.

VCO gets DC in, puts out a frequency. Say we are running at 10 MHz. How can I make it lock to some other 10 MHz output so that the VCO is always outputting 10 MHz? There is some variation due to heat, voltage variation, other factors. Government built a clock from radiation decay that is a standard and the output of which is transmitted on station WWV at various frequencies like 10 MHz.

Phase Comparator

Phase comparator is the circuit that does this. Compares the phase of the WWV signal to the phase of the locally generated signal. Adjusts the DC level.

How does a phase comparator do this? XOR gate will do this. Truth table:

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

The two input waveforms are square waves at TTL voltages. As long as the waveforms are different, the XOR gate outputs a 1, and outputs a 0 when they are the same. An XNOR gate would output a 0 when different and 1 when same.

Take a phase detector (phase comparator detector). One input is WWV. The other input is fed back from the output of the VCO. This detector is more complex than an XOR gate. Output of detector is fed through a filter. Why? The filter is an integrator; it outputs a larger signal when the difference is greater and a smaller signal when the difference is small. Diagram 3.

Phase detector generates DC proportional to the amount of phase difference. This will change the VCO frequency. Actually, not changing frequency as much as changing the phase. That's why it's called a phase locked loop, not a frequency locked loop. The output voltage of the comparator/filter is the **error voltage** resulting from the differences between the two signals.

Diagram 4.

Testing these, the engineer may have a specific reference voltage at a test point. These PLLs work very well unless there's something very wrong.

Suppose receiving a station at 105.9 MHz. FM. Can make an FM detector out of a phase locked loop, since the output voltage will change according to the frequency. The correction voltage outputted is the audio waveform.

One of the biggest challenges as a tech is troubleshooting a VCO. If one thing stops working, it's tough to troubleshoot unless you understand how VCOs work. For example, new Sony cameras use a PLL in the CCU system. The oscillator is in the camera head and the detector is in the CCU.

PLLs came around in the 1950's. Used in TVs. Vertical hold and horizontal hold. Oscillator was not that stable, would have to readjust at least once in an evening of viewing. Didn't have a VCO then, but started to put PLLs into TVs since people complained about having to readjust holds.

Remote controls used to be mechanical/ultrasonic.

Suppose have a stable WWV signal as input. Want to lock it to 20 MHz to make a stable clock. Could use a frequency doubler to double the input before feeding it into the PLL. Could also divide by 2 using a flip-flop on the feedback leg out of the VCO and feed that to the comparator.

If have a selectable divide-by system on the feedback line in the PLL. Will find this on audio generators, RF generators. Today called synthesizers. Generating the frequency we are telling it to based on our reference. The input could be a precisely-cut crystal, oven temperature controlled.

We do this downstairs in lab. Our input frequency is 2400 Hz for the time code reader. Our goal is to produce 9600 Hz. Must divide output by 4 to get that to feed back to the comparator. Detects Manchester encoding by seeing if the pulse is wide or narrow. Goal is to have the 9600 Hz signal start and stop within the frame of 2400 Hz Manchester-encoded time code coming in.

A **pull-in limit** is the limit to which the PLL can correct a frequency.

Using a 4046 PLL chip for the time code reader.

As we pull tape through a VTR, must ensure tape is in line with head. A PLL can change the phase of where the tape is placed. Moving the tape back and forth to ensure adjusted to beginning and end of video track.

PLL is an analog circuit that uses square waves to function. There are digital PLLs today that doesn't use any analog components.

Phase Detector

The phase detector is also analog. Could use the 7486 XOR. Another way to do it. Take the WWV signal. Take a ramp/sawtooth wave (used for deflection in monitors). Generate this sawtooth waveform based on the input frequency. One input is the reference, the other is the VCO output. The output of 20 MHz may be out of phase. Pass feedback through divide by 2 to get 10 MHz back.

Ramp and Sample

Ramp goes from 0 to 5 volts. If sample a voltage at a specific point in the ramp by differentiate (Steve says integrate) this, get a sharp pulse. Will at most sample once per cycle. Can sample less often to in

effect have a divider (like sampling every 2 cycles, or every 10 cycles).

The spike generated from sampling of the ramp is stored in a capacitor, and is used to output to the VCO to control the VCO in order to change where within the ramp the sample is taken. Sample will move up and down the ramp until it finds the desired voltage. This will only require one cycle if the input signal has a stable frequency.

Looking for a 4.5 VDC **quiescent** result in this example. Gradually gets to 4.5, starts feed back to tell Diagram 5.