# Manchester Encoding

Used in SMPTE time code. (Differential) bi-phase is another name for it.

First published in 1949. A synchronous clock encoding technique. The clock is encoded into / embedded in the signal. Used to encode the clock and data of a synchronous bit stream.

In this technique, the actual binary data to be transmitted are not sent as sequence of logic 1's and 0's. Instead, the bits translated into slightly different format that has advantages over straight binary encoding.

Diagram 1. Transition between states in the middle signals the one, no transition signals a zero. Depends on the change from one voltage to the other within a cycle. Why do this? If send a bunch of zeroes or ones in a row in straight binary, lose the embedded clock. Changing the voltage level at period/cycle boundaries, regardless of the value being encoded, embeds the clock in the value. Transmitting a long string of 1s or 0s means that DC is sent, which can have a voltage drop. This encoding is considered AC since it changes state at least once every clock cycle.

## *Manchester Encoded Signal*

Contains frequent level transitions which allow the receiver to extract the clock signal using a Digital PLL (phase locked loop (DPLL)) and correctly decode the value and timing of each bit.

To allow reliable operation using DPLL, transmitted bit stream must contain high density of bit transitions. Manchester encoding ensures this, allowing the receiving DPLL to correctly extract the clock signal.

The penalty for introducing frequent transitions, is that the Manchester encoded signal consumes more bandwidth than the original signal (in NRZ – not return to zero).

Bi-phase Manchester encoding can consume up to twice the bandwidth of the original signal.

If look at signal coming in from time code generator, it goes above and below zero. Can transmit farther this way over a line. We convert it to 0 and 5 volts for TTL chips; going below zero volts on TTL could damage chips. Using 1 V p-p downstairs; this may be the standard. That's why we have to boost the voltage to 5 volts.

Diagram 2.

Output of our common emitter configuration is 180 out of phase (inverted); doesn't matter to Manchester encoding.

# Phase Locked Loop

What is heart of a PLL (phase locked loop)? The VCO (voltage controlled oscillator). It produces a frequency. Controlled by varying voltage on the input. Changes the voltage across the varactor diode, which changes its capacitance. Has a filter before the VCO, then a phase detector before that. VCO outputs 19,200 Hz. Divide by 8 circuit on feedback means that supplies 2400 Hz; that's what the input frequency must also be. Will see why later why we run at 19,200 Hz and not just 2400 Hz.

Continually reads the frequency, compares it, and adjusts. The VCO has an RC time constant built in;

would have to change a resistor and a capacitor to define the frequency.

What does it mean that the 19200 Hz is locked to the 2400 Hz? Both are in phase with each other. These are both square waves. Transitions of the 2400 Hz occur at a transition of the 19200 Hz. Diagram 3.

Where is a good place to sample? On the rising edge. Some chips are edge-triggered. 7474 D flip-flop (delay or data) is edge-triggered by the clock input (on the rising edge of the clock, whatever is on D is transferred to Q). Diagram 4. Sample the 2400 Hz wave on the rising edges of the 19,200 Hz wave. Use a higher frequency clock so can sample somewhere in the center of the data, so that if it moves (jitters – a phase shift often caused by noise on the line).

### *Jitter*

Diagram 5. Noise can widen the leading edge so that the edge triggering can occur within a range of times. Chips often handle this due to designing to the specifications by which they are built.

Oscillator is a resonant circuit that keeps getting positive feedback to maintain its oscillations.

### *Phase detector*

Generate a ramp from -2 to 2 volts. Resets every time we hit a trailing/falling edge. Using a small part of the capacitor range since we want a linear portion of the RC curve.

Diagram 6. Object is to center the ramp at ground. Sample voltage at the middle of the ramp. If frequency increases, shifts over and shortens the ramp. Finds out that there is a higher voltage at the sampling time, so it tells the VCO to slow down. Opposite would happen if frequency decreases (lengthens the ramp, see lower voltage at sampling time). Ramp moves around but the time at which the sample is taken does not.

### *Filter*

What does the filter do? Very important. Smooths the signal. Want the VCO to make gradual changes, not sudden changes. Gradual within two or three samples. Uses a capacitor and a resistor. Just respond to real trends not blips.

## Lab

4046 PLL. They are used a lot in the equipment that we use.

How the VCO works, how the filter works. Will build as part of time code reader.

Nomograph. Diagram 7. Manufacturers chart all calculations on a graph. Along the graph they have the components you'd want to select, e.g., for 5 volts, limit resistor choice between 1 and 10 K and limit capacitor choice between some other range.